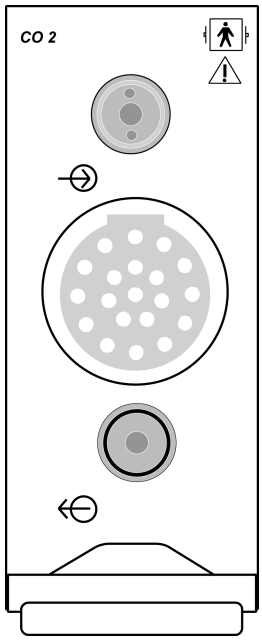
CO2 MODULE

INTRODUCTION

This area contains component information about the Model 7345 CO2 Module. The CO2 Module monitors the partial pressure of respiratory carbon dioxide. It measures the absorption of infrared light by respiratory gases and calculates endtidal carbon dioxide (ETCO2) and inspired CO2. A sampling pump allows monitoring of a mainstream or sidestream sample of airway gases. Respiration rate is calculated by measuring the time intervals between peaks of the CO2 waveform. The displayed rate is the result of averaging the inverse of the 8 most recently detected time intervals.

The CO2 Module provides automatic compensation for the effect of barometric pressure on the CO2 reading, user-selectable compensation for the presence of more than 60% oxygen and the presence of more than 50% nitrous oxide, and the ability to modify the detection algorithm to compensate for artifact-induced waveforms.



PHYSICAL DESCRIPTION

The CO2 Module is shown in FO-7B. The Module contains a front panel with one patient connector and sampling pump inlet and outlet, a flex PWA, an OEM PWA, and a digital/power supply PWA. The flex PWA provides power and signal connections from the OEM PWA to the front panel sensor connector.

FUNCTIONAL PRINCIPLES OF OPERATION

A functional block diagram of the CO2 Module is shown in FO-7A. The diagram is divided into isolated circuitry and non-isolated circuitry. The isolated circuitry includes the CO2 sensor, the flex PWA, and the OEM PWA. The isolated (ISO) interface and push-pull transformer isolate this circuitry from the non-isolated core logic. The core logic provides communication between the system host and CO2 Module through the PNet synchronous serial interface. It also controls data acquisition and data processing functions for the CO2 monitoring channel.

Isolated Circuits

Isolated circuits are shown in the top half of FO-7A. The sampling pump receives power from the OEM PWA through the front panel connector. Power from the Module is applied to an infrared (IR) light emitter in the CO2 sensor. The signal from an IR receptor in the CO2 sensor is received through the front panel connector and is connected to the OEM PWA via the flex PWA.

The isolated interface provides an isolated asynchronous serial communication channel between the core logic and the OEM PWA. The isolated power block consisting of isolated +12V, +5V, and two -12V power supplies provides isolated power to the OEM PWA and the sensor connected circuitry.

Non-Isolated Circuits

Non-isolated circuits are shown in the bottom half of FO-7A. Functional blocks include the PNet interface, pulse width modulator (PWM) and power switcher, isolated power control, reset/failsafe, 68302 CPU, 128Kx8 data memory, 128Kx8 program memory, the model and serial number EEPROM, and logic analyzer/test interface.

Power (+12V and +5V), is received through J1. The +12V is applied to the PWM and power switcher that powers the isolated circuitry. ISO power control

limits the PWM power-on until after the CPU is reset and shuts down the PWM if a failsafe condition occurs.

The Module will not be damaged when plugged into a live slot. Core logic power inputs to a Module are limited to a peak inrush current during hot-plugging. Within 2 seconds the Module responds to identification and wakes up in a minimized power state until registered with the system.

The PNet interface allows asynchronous and synchronous data transfer between the core logic and the external devices. Synchronous operation is always used in MPS systems. Asynchronous operation is for test and development only. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafe if a problem occurs with the microprocessor. The microprocessor controls and transfers data within the core logic. The program memory is a FLASH device that can be loaded with program information from the PNET interface or the logic analyzer interface. Data memory temporarily stores status and monitoring data for processing.

COMPONENT PRINCIPLES OF OPERATION

Schematic diagram SC315-446 is provided. The first sheet of the schematic shows an overall block diagram of the CO2 digital PWA.

CO2 Front End

The EMI filtering at the CO2 front end connector is provided in a flex PWA (313-103) which contains a common mode ferrite core and 100 pF bypass capacitors on each signal pin of J2. The flex PWA is also shielded. Signals are sent and received through front end connector J2 with the following pin-out:

PIN	NAME	PIN	NAME
1	SRC+	11	EEDIN
2	SRC-	12	SPANSW
3	EECS	13	SRC_SHEILD
4	REF_IN	14	ZERO_SW
5	CASE_HTR	15	CASE_THRM
6	CO2_IN	16	DET_HTR
7	EESK	17	DET_THRM
8	HTR_RTN	18	-12CAPNO
9	EEDOUT	19	+12V
10	VDD	20	AGND

OEM PWA

The OEM PWA is a self-contained CO2 detection system. It has no serviceable parts, and must be returned for repair.

Isolated Power

The isolated power section provides patient isolation from earth ground by isolating the power for the patient connected circuitry. The isolated power supply is shown on sheet 7 of the schematic.

Pulse Width Modulator (PWM) U102 drives the FET power switchers Q101, Q102 for push-pull transformer T101. The PWM senses primary current via feedback resistor R112. The transformer has one center-tapped primary side and two center tapped secondary sides with nominal output voltages of 6.1V and 15.9V.

Short-circuit protection for the isolated power supplies is provided by the pulse-to-pulse current limit feature of the PWM. Resistor R112 senses the current through power switchers Q101 and Q102, R116 and C122 filter out the switching spikes in the voltage across R112, and resistors R114 and R115 set the current limit value of the PWM. The PWM will function normally once the short is removed.

The PWM is synchronized to the Core Logic clock (200 KHz) by TIMER2 output from the CPU. Removing R143 allows the PWM to free run asynchronously at approximately 100KHz.

The output of the PWM is the logical OR of FS-1 and ISO_PS_ON-0. During power-on, ISO_PS_ON-0 remains pulled up until the CPU comes out of the reset state. During failsafe conditions, FS-1 is asserted, and the ISO_PS is shut down.

The 6.1V from the secondary of push-pull transformer T101 is bridge rectified by CR101 and CR102 to give approximately +5.3Vdc. This voltage is then regulated using U101a and controlled power FET Q109 to give +5Vdc (ISO_+5V). Op-amp U101 gets a precision reference of +5V from REF02 U105.

The 15.9V from the secondary of isolation transformer T101 is bridge rectified by CR103 and CR104 to give approximately+15Vdc, and CR105 and CR106 to give approximately -15 Vdc. The +15Vdc is regulated by op-amp U104a and controlled power FET Q105 to give regulated +12Vdc (ISO_+12V). The +12V regulator gets a precision reference of +5V from REF02 U105. The -15Vdc is regulated by op-amp U104b and controlled power FET Q104 to give regulated -12Vdc (ISO_-12V1). A second, independent, low power -12V output (ISO_-12V2) is implemented with regulator U106.

Op-amp U104b used in the -12Vdc regulator gets a non-inverting input from instrumentation amplifier U103, which scales the difference in voltage between the +12V and -12V outputs to a 4.9V nominal output. Window comparators U112a and U112b generate POWER_GOOD when the output of U103 is 4.9V ±2%. POWER_GOOD from U112 is sent back to the Core Logic CPU via optocoupler U110. If the output from U103 falls out of the 4.9V ±2% range, POWER_GOOD goes false and signals the Core logic CPU to shut down the power supply.

Isolated Interface

As shown on sheet 7 of the schematic, opto-couplers U107 and U108 provide a full duplex, isolated serial channel between the non-isolated core logic and the isolated circuitry as ISO_DATA_IN and ISO_DATA_OUT. Q107 and Q108 buffer the signal to the opto-couplers. U110 couples the POWER_GOOD signal across the isolated interface.

Core Logic

The core logic is shown on sheets 2 through 6 of the schematic. The core logic provides communication between the system host and Module through the PNet synchronous serial interface. It also controls data acquisition and data processing functions for the CO2 sensor. The Module is an 8-bit version of the core logic with one 128Kx8 RAM and 128Kx8 ROM device. The microprocessor runs at 9.869 MHz.

PNet Interface

The PNet interface, shown on sheet 2 of the schematic, provides the following functions:

- RS485 drivers (U7 and U8) for serial data and clock,
- Module select and presence detection (U2),
- Module synchronization.

Core signals are received on PNet connector J1 (sheet 1) with the following pin-out:

PIN	NAME	PIN	NAME
1A,1B	+5V	6B	M_SELECT
2A	DATA+	7A	M_PRESENT
2B	DATA-	7B	TXOC-0
3A,3B	+3.3V	8A	M_SYNC-0
4A	CLK+	8B	-12V
4B	CLK-	10A,10B	+12V
5A,5B	GROUND	1,2	GROUND
6A	M_RESET		

The CO2 Module is designed to be inserted and removed ('hot-plugged') from powered systems. Ground pins 1 and 2 are longer than the other connector pins, thus they make first and break last to protect the circuitry. This is partially because of protective impedance located on the system backplane, in series with the modules +5V and +12V power. Also series impedance on PNet control lines limits inrush and protects logic devices from excessive currents during a hot-plug power up.

The PNet protocol defines two modes of operation: synchronous and asynchronous. The normal mode of operation is synchronous, with half duplex transmitted and received data on differential signals DATA+ and DATA-. As shown on sheet 2 of the schematic, the device transmitting the serial data also generates differential clock signals CLK+ and CLK-. Transceiver direction for data and clock are controlled by the 68302 processor-generated TX_EN-0 (low true transmit enable) signal through U2. In the synchronous mode, both data and clock transceivers U7 and U8 are set to receive (i.e., transmit disabled) when fail-safe signal FS-0 is asserted.

The alternate serial mode, full duplex asynchronous, is entered by asserting processor generated control bit ASYCH_EN. This mode transmits data onto the differential signals CLK+ and CLK-, and receives data from the differential signals DATA+ and DATA-. The transmitter in the Module is disabled unless the Module has been commanded to transmit per the PNet protocol. The Module transmitter is immediately disabled after the last character of a transmission has been sent.

The Module select input (M_SELECT, hi true) instructs the Module to respond to identification requests. When both M_SELECT input and M_RESET input (hi true) are asserted, the Module performs a hardware reset.

The Module present output, M_PRESENT is connected to M_SELECT through diode CR1 to allow a means of determining if the Module is plugged into an instrument. When M_SELECT is asserted (pulled hi) M_PRESENT is hi true.

Module transmitter open collector signal TXOC-0 from Q1 signifies the Module transmitter is enabled. Serial data is then transmitted in the synchronous mode.

M_SYNC is used for timing of shorter latency periods than supported by the serial data protocols. A Module only asserts M_SYNC when enabled by the host.

Reset Logic

The reset logic is shown on sheet 3 of the schematic. Reset logic U9 generates a power-on-reset when power is applied. RESET-0 AND HALT-0 signals remain low for minimum of 130 msec after all logic voltages are in specification.

External reset, processor reset, and halt signals are low for minimum of 24 clocks when external reset asserted. Power monitoring, processor reset, and halt signals are low if logic voltages drop below specification. They remain low for minimum of 130 msec after logic voltages return to the specified range.

The reset circuit consisting of U6b and U6d provides open drain outputs to the processor bi-directional reset and halt signals.

Fail-Safe Logic

Fail-safe latch (U6a and U6c) ensures that the Module enters a safe state if the processor fails to operate correctly. The latch is set by a low true output from the processor watchdog timer (WDOG-0). The data transmitter is disabled, isolated power is shut down, and the Module remains in a safe state until the latch is cleared by a power on or external reset.

Microprocessor

The core logic design is based around the 68302 microprocessor (U10) shown on sheet 4 of the schematic. The 68302 combines a 68000 core with a three channel communication processor, and system integration circuits.

The left side of the CPU contains clock interfaces to/from the PNet, port A, and port B to various circuits in the core logic, reset, and halt interface. The IRQ ports are not used. The right side of the CPU contains address and data lines and chip select outputs. The 68302 operates with a statically defined 8-bit wide bus. The following resources are used for specific Module functions:

CHIP SELECTS LOGIC

CS0-0	FLASH ROM
CS1-0	STATIC RAM

SERIAL COMM CHANNELS

SCC1	PNET [RXD1, TXD1, RCLK1, TCLK1, CTS1-0, RTS1-0]
SCC2	ASYNC DEBUG [RXD2,TXD2]
SCP	SERIAL EEPROM [SPRXD,SPTXD,SPCLK]
TIMER1	SYSTEM TIMEBASE

PARALLEL IO / SPECIAL PURPOSE IO BITS

PA2	CHIP SELECT TO SERIAL EEPROM
PA5	ASYCN_EN (PNET MODE SELECT)
PA6	POWER MANAGEMENT CONTROL
PB5 /TIN2	TIMEBASE INPUT FOR EXTERNAL MEMORY / SYSTEM CONFIG
PB7	WATCHDOG TIMER OUTPUT

Program Memory

Program memory consists of 8-bit flash ROM U11 shown on sheet 5 of the schematic. The ROM is configured for 128Kx8 (1024k bit). The ROM is not socketed and can not be removed for programming. The ROM can be flash-programmed via the logic analyzer interface or the PNET connector.

Data Memory

Data is stored in 128Kx8 static RAM U3 shown on sheet 5 of the schematic. This RAM is cleared when power is removed.

Non-Volatile Memory

Serial EEPROM U1 shown on sheet 5 of the schematic is a 128-byte PROM that provides non-volatile storage for model and serial number information and parameter user interface data which must travel with the Module. The 68302 synchronous communication port (SCP) is used to access the EEPROM.

Logic Analyzer/Test Interface

The logic analyzer/test interface is shown on sheet 6 of the schematic. The core logic includes an interface to bring signals required for external ROM access, logic analyzer interface, and a debug serial channel to a single connector.

The external ROM access allows an off board ROM (8 bit) or ROMs (16 bit) to replace the FLASH devices at address 0. Address, data, and control signals required for this function are included on the LA/T connector.

All signals needed for a Hewlett Packard model 16500 logic analyzer or equivalent to perform bus state analysis and disassembly are included on the LA/T connector.

The 68302 SCC2 serial transmit and receive data signals are included on the LA/T connector.

The LA/T connector pinouts are as follows:

PIN	NAME	PIN	NAME
1,69	+5V	2,28,45,46,70	GND
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
29	D0	30	D1
31	D2	32	D3
33	D4	34	D5
35	D6	36	D7
37	D8	38	D9
39	D10	40	D11
41	D12	42	D13
43	D14	44	D15
47	DTACK-0	48	AS-0
49	RW	50	UDS-0
51	DS-0	52	BGACK-0
53	FC0	54	FC1
55	FC2	56	DEBUG TXD
57	DEBUGRXD	58	EXROMCS-0
63	PRGM_EN	64	DISCPU
65	T1_IN		

DISASSEMBLY PROCEDURE

STATIC DISCHARGE CAUTION

Do not attempt to service unit without static discharge protection. Workstations and personnel must be properly grounded, or damage to equipment will result.

1. Remove two 4-40 x 5-1/4" screws from the rear of the Module. Remove rear cover.
2. Slide enclosure toward rear of Module, and remove enclosure.
3. Remove insulators.
4. Pull two card guides away from PWA and shield assembly, and remove guides.
5. Carefully separate digital PWA connector and shield assembly at top of Module.
6. Remove tubing from inlet of pump.
7. Remove tubing and wire wraps from outlet of pump.
8. Remove pump connector from OEM PWA.
9. Remove 4-40 screw that secures flex assembly to OEM PWA. Remove flex assembly by pulling it upward.

10. Disassemble OEM shield assembly by disengaging each of the corner locking tabs (accessible through plastic shield vent openings)

11. Using FO-7B as a guide, perform any additional disassembly that may be required for maintenance procedures.

REASSEMBLY PROCEDURE

1. Make sure that fastening tabs on emi shield cover (44, FO-7B) for OEM PWA have not been deformed. Reassemble OEM PWA and shield assembly.

2. Secure pump. Push upper hose with filter onto pump inlet. If outlet tube was removed from barbs, push lower hose onto pump and replace wire ties.

3. Install front panel flex PWA connector and secure with 4-40 screw (43) and lock washer (50). Route pump wires under flex stiffener as shown in View A of FO-7B, to ensure integrity of patient safety isolation.

4. Install digital PWA in front panel slot, and connect 10-conductor interface connector.

5. Carefully hold PWA and shield assembly together, and push upper and lower card guides onto slots. Install insulators.

6. With enclosure oriented so large groove is at bottom and label is at right (viewed from front of Module), slide enclosure over PWAs and shield assembly.

7. Install back cover on the Module enclosure.

8. Fasten the front and rear covers to the enclosure by inserting two 4-40 x 5-1/4" screws from the rear through the enclosure to the front cover as shown in FO-7B. Tighten the two screws to 4-in/lb.

SAMPLING SYSTEM CLEANING PROCEDURE

Whenever required, perform the steps listed below to clean and sterilize internal sampling system components. Compatible cleaning and disinfecting solutions are:

- Chlorine bleach disinfectant, 5.25%, various brands, 0.75 cup per gallon of water
- Isopropyl alcohol
- Cidex Formula 7® or pHisoHex®
- Quatenary-based germicidal detergents like VESTAL INSURANCE®, HI-TOR PLUS®, or VIREX®

For the above, follow manufacturers' recommendations for dilution rate and use. These recommendations are not an endorsement of the manufacturers or of the effectiveness of these materials for cleaning or disinfecting.

CAUTION

Do not attempt to pump cleaning and sterilizing liquids using the sampling pump. This may cause accelerated wear on the pump bearings. Always flush liquids with a syringe, as described below.

1. Turn off the Monitor and disconnect the power cord.

® Cidex Formula 7 is a registered trademark of Johnson & Johnson Medical Products, Inc. pHisoHex is a registered trademark of Winthrop-Breon Laboratories. VESTAL INSURANCE is a registered trademark of the Vestal Corp. HI-TOR PLUS is a registered trademark of the Huntington Corp. VIREX is a registered trademark of S.C. Johnson & Son Corp.

2. Remove both the sampling inlet tubing set and the sampling exhaust tubing, if any.

3. Attach an exhaust port line (1/8 inch ID tubing or 3/16 inch ID tubing) from the sampling exhaust port to a suitable container located below the bottom level of the Monitor.

4. Fit a 60 cc catheter tip syringe to the sampling inlet connector. Flush the sterilizing solution slowly through the pumping system. Push the entire 60 cc of solution through the inlet. Repeat this process twice, until about 180 cc of solution is used.

5. Remove the syringe, and leave the cleaning or sterilizing fluid within the sampling pump system for 30 minutes (for a disinfectant), or for as long as recommended by the manufacturer if a sterilizer is used.

6. After 30 minutes, fill the syringe with distilled water and flush the system three times. Allow the cleaning or sterilization solution and distilled water to drain through the sampling exhaust outlet.

7. Push several syringes of air slowly through the system to ensure that most of the liquid has been drained.

8. Follow this with at least three more flushes of distilled water, then push through at least two syringes of air to ensure most of the distilled water has been drained.

9. Remove the syringe from the unit. While the sampling inlet tubing is still disconnected, connect the Monitor power cord and power it on. Allow the sampling pump to operate for several minutes. This will help to remove any trapped water.

10. Connect a sampling tube set to the sampling inlet.

11. Block the open end of the tubing with your finger. Alternately block and clear the tubing at least ten times, each time for several seconds, using a quick, brisk motion.

12. Block the open end of the sampling exhaust port, and block and clear this port in the same way described above.

13. To speed up drying the system pneumatics, allow the sampling system to run without any sampling inlet or exhaust tubing for at least 30 minutes.

PARTS LISTS

Top Assembly 7345 parts are listed in Table 7-1 and shown in FO-7B. CO2 Digital PWA 315-446 parts are listed in Table 7-2 and shown in FO-7C.

Table 7-1. Top Assembly 7345 Parts List

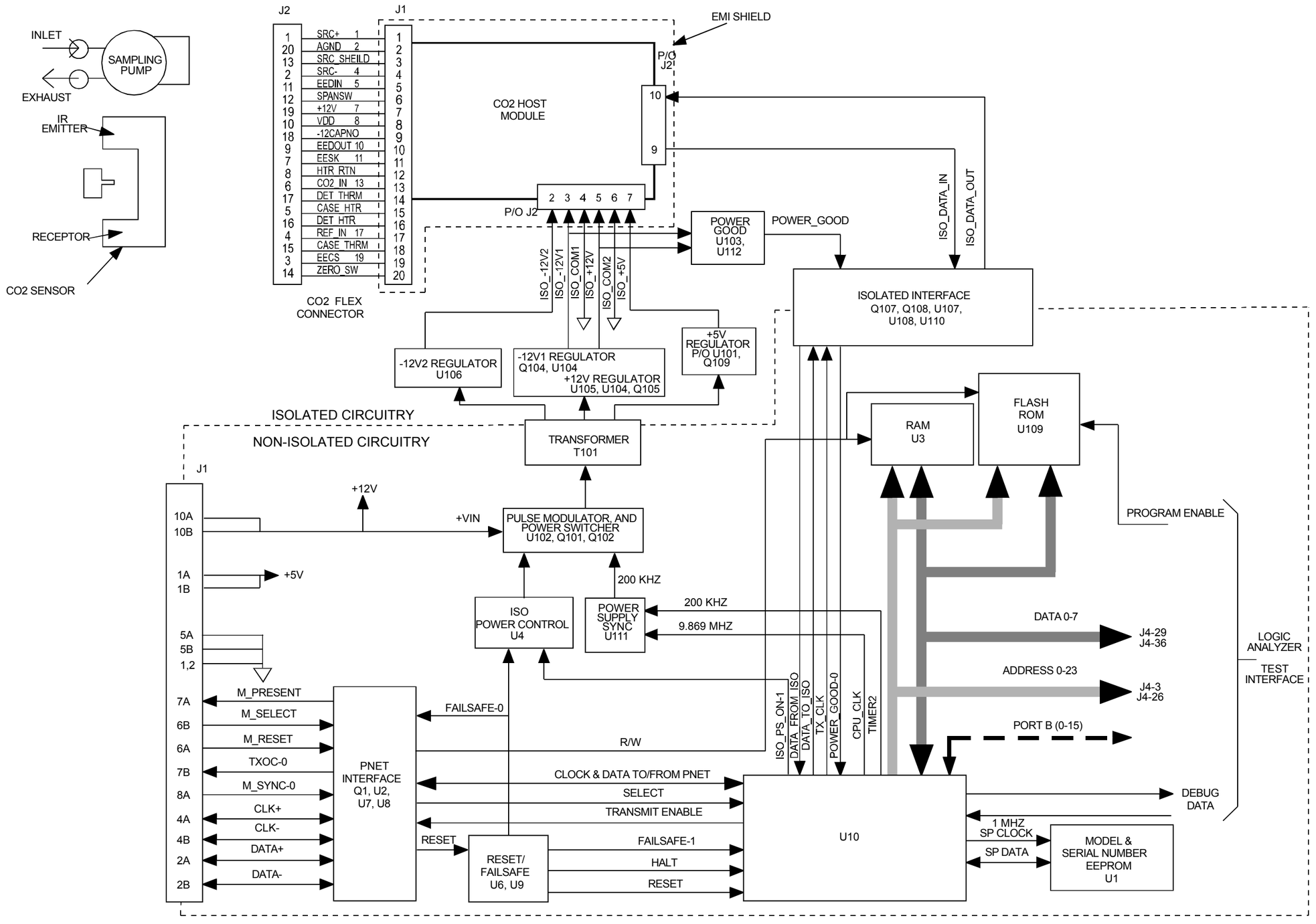
Item	Description	Part No.
1	COVER, PARAMETER REAR	703-188
2	SUB-ASSY, ENCLOSURE, EXTRUDED SW	320-676
3	PANEL, FRONT, C02	701-416
4	PWA, FLEX, FRONT PANEL, C02	313-103
5	TUBING PHARMED	740-185
6	FILTER, AIR,43 MICRON STAINLESS FILTER	754-136
7	HOSE BARB FITTING	754-120
8	LUER, FEMALE	712-256
9	HOSE BARB, ADJUSTABLE	754-145
15	PWA, C02 DIGITAL	315-446
19	SCREW, RDH PHH, 4-40X51/8, CUSTOM	722-201
20	INSULATION, GUIDE, MODULE	750-182
22	SCREW, 2-56X3/16 PNH PHH SST	719-237
24	SCREW, 4-40X1/4 PNH PHH SST	719-102
26	BUTTON, LATCH, SW	732166
27	SPRING, CONTACT, GROUND	736-204
30	GASKET, CONNECTOR, C02	703-193
33	NOVA/SHIELD ASSY	320-669
34	INSULATOR, DIGITAL	750-189
36	FITTING,TUBE,NYLON	712-268
37	TUBING POLYURETHANE 5/32 0D X 5/64 ID	740-197
38	INSULATOR, NOVA, CAN	750-191
39	PUMP,AIR,12V DC MOTOR	712-265
40	SCREW,2-56X3/16 100DEG FH	719-239
41	PAD, MOTOR MOUNT	752-266
43	SCREW, 4-40X3/8 PNH, PHH,SST	722-229
44	SHIELD, EMI, METAL C02	737-183
45	PWA, CO2 OEM, NOVAMETRIX	645-171
46	TYWRAP NYLON .75 BDL DIA.MAX.	756-101
47	TUBING,TYGON 3/32 ID X 5/32 OD	740-199
48	TUBING,TYGON 3/16 ID X 1/4 OD	740-200
49	INSULATOR, NOVA PWB	750-192
50	WASHER, LOCK, FL-INT TOOTH SST # 4	724-106
51	WASHER, LOCK, FL-INT TOOTH # 2	724-115

Table 7-2. CO2 Digital PWA 315-446 Parts List

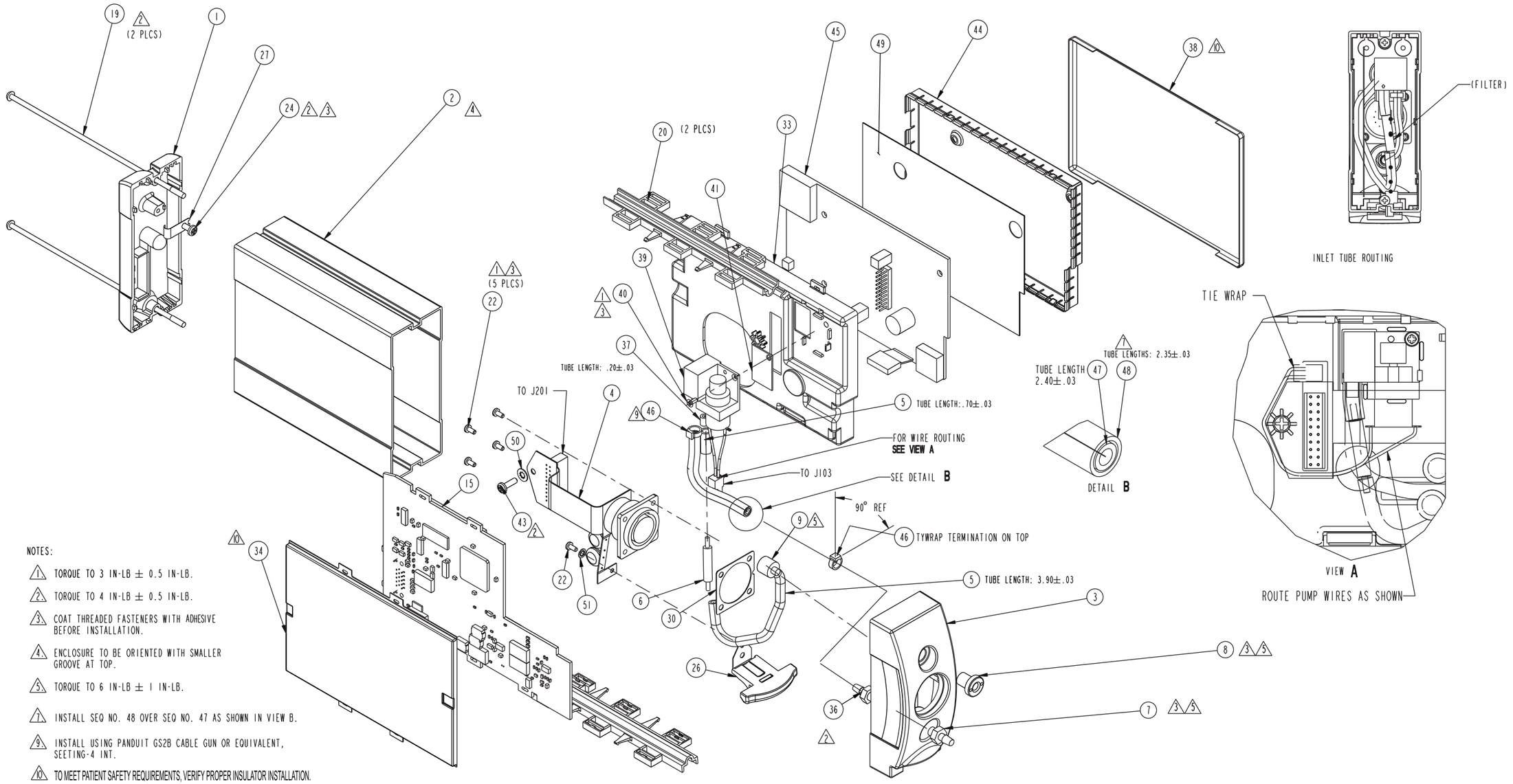
Item	Description	Part No.
C1	CAP,2917/D,TANT,35V,20%,10 UF	606-188
C2,C3	CAP,CER,SMD,0603,NPO,10%,50V,27 PF	605-718
C4-16,101-107, 109,110,112, 121,125-128, 134,135	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C111,113-115	CAP, ELCTLT, 100 UF, 16V, SMD	604-191
C117-119,129	CAP, ELCTLT, 68 UF, 35V, SMD	604-190
C120	CAP,CER,SMD,0603,NPO,10%,50V,220 PF	605-729
C122,124	CAP,CER,SMD,0603,X7R,10%,50V,1000 PF	605-809
C130,131,133	CAP,CER,SMD,0603,Z5U,20%,50V,0.033 UF	605-919
CR1,13	DIODE, SCHOTTKY, 30V, 200MW, SOT-23	611-137
CR2-7,10,11	DIODE, DUAL SERIES SMT SOT-23	611-140
CR12	DIO ZENER 6.2V, 5% SMT, 225MW	612-147
CR101-106	DIODE, RECT-SCHOTTKY, 3A, 40V, SMT	611-145
FB1-9,100	FERRITE CHIP, EMI SUPPRESSION, SMT	669-170
J1	CONN, 20 PIN PLUG RT ANGLE PC MOUNT	607-795
J2	CONNECTOR, 10 CONDUCTOR	608-344
J4	SOCKET, MICRO STRIP 35X2, SMD	607-816
L101	INDUCTOR, 10UH 20% 2.6A 0.06 DCR SMD	669-205
Q1	XST NPN 2222A SMT	674-127
Q101,102,104, 109	XSTR, POWER FET, TMOS, N-CHANNEL DPAK	676-157
Q105	XSTR, PWR, NPN, DARLINGTON SMD	673-116
Q107,108	XST PNP SMT	674-126
R1,40,41,44,50, 128,130	RES,0603,1/16W,1%,1.00K OHM	686-293
R2	RES,0603,1/16W,1%,4.99K OHM	686-360
R3,4,7-33,35, 42,43,46,47,48, 102,111,117	RES,0603,1/16W,1%,10.0K OHM	686-389
R5,6,126,129, 144	RES,0603,1/16W,1%,2.21K OHM	686-326
R34	RES,0603,1/16W,1%,698K OHM	686-566
R45	RES,0603,1/16W,1%,100 OHM	686-197
R105,106,110, 121,122	RES,0603,1/16W,1%,10.0 OHM	686-101
R107,108	RES,0603,1/16W,1%,100K OHM	686-485
R112	RES,2512,1W,1%,0.1 OHM	686-607
R113	RES,0603,1/16W,1%,12.7K OHM	686-399

Table 7-2. CO2 Digital PWA 315-446 Parts List (Continued)

Item	Description	Part No.
R114	RES,0603,1/16W,1%,49.9K OHM	686-456
R115	RES,0603,1/16W,1%,20.0K OHM	686-418
R116	RES,0603,1/16W,1%,1.40K OHM	686-307
R118,120,135	RES,0805,1/10W,0.1%,21.5K	685-629
R119	RES,0805,1/10W,0.1%,11.0K	685-630
R123	RES,0805,1/10W,0.1%,3.57K	685-628
R124	RES,0805,1/10W,0.1%,4.99K	685-623
R127,131,141	RES,0603,1/16W,1%,750 OHM	686-281
R132	RES,SMD,1/10W,JUMPER 0.0 OHM	685-606
R133,134	RES,0603,1/16W,1%,442 OHM	686-259
R136,137	RES,0603,1/16W,1%,6.04K OHM	686-368
R138,140	RES,0603,1/16W,1%,1.0M OHM	686-581
R142,143	RES,0603,1/16W,JUMPER 0.0 OHM	686-606
T101	XFORMER, POWER HI-FREQUENCY, TOROID	668-164
U1	IC,93C56 2KBIT SERIAL EEPROM,CMOS SM	692-183
U2	IC, EECMOS PLD 16V8B, ARRAY LOGIC	692-226
U3	IC, 128X8 70NS CMOS SRAM TSOP	694-133
U4	IC,74AC32 QUAD 2 IN OR GATE,ADV CMOS SM	692-141
U6	IC,74HC03 QUAD 2 IN.NAND,CMOS SUF MT	692-139
U7,8	IC, CMOS LTC1485, DIFF BUS XCEIVER SO8	692-225
U9	IC, POWER SUPPLY MONT WITH RESET SMT	694-118
U10	IC, 68302 INTEGRATED PROCESSOR 144 SMT	694-130
U101,104	IC, OP-AMP, DUAL/QUAD, PRECISION SMD	691-141
U102	IC, LO-POWER, PWM, CURRENT MODE SMD	693-166
U103	IC, AD620BR, INSTRUMENTATION AMP, SMT	692-187
U105	IC, 5V REG/TEMP XDCR, SMD	693-121
U106	IC, -12V VOLTAGE REG SOIC	693-167
U107,108,110	IC, HCPL-2611, OPTOCOUPLERS, SMT	695-101
U109	IC, 128K X 8-BIT 5V FLASH ROM CMOS SMT	692-195
U111	IC, SMT, DUAL D FLIP FLOP	692-117
U112	IC, DUAL COMPARATOR SMD	693-158
Y100	CRYSTAL, 9.869MHZ, 0.005% HC-49UP	609-129
#16	PAL_U2A, CORE LOGIC	637-101



FO-7A. CO2 Module Block Diagram



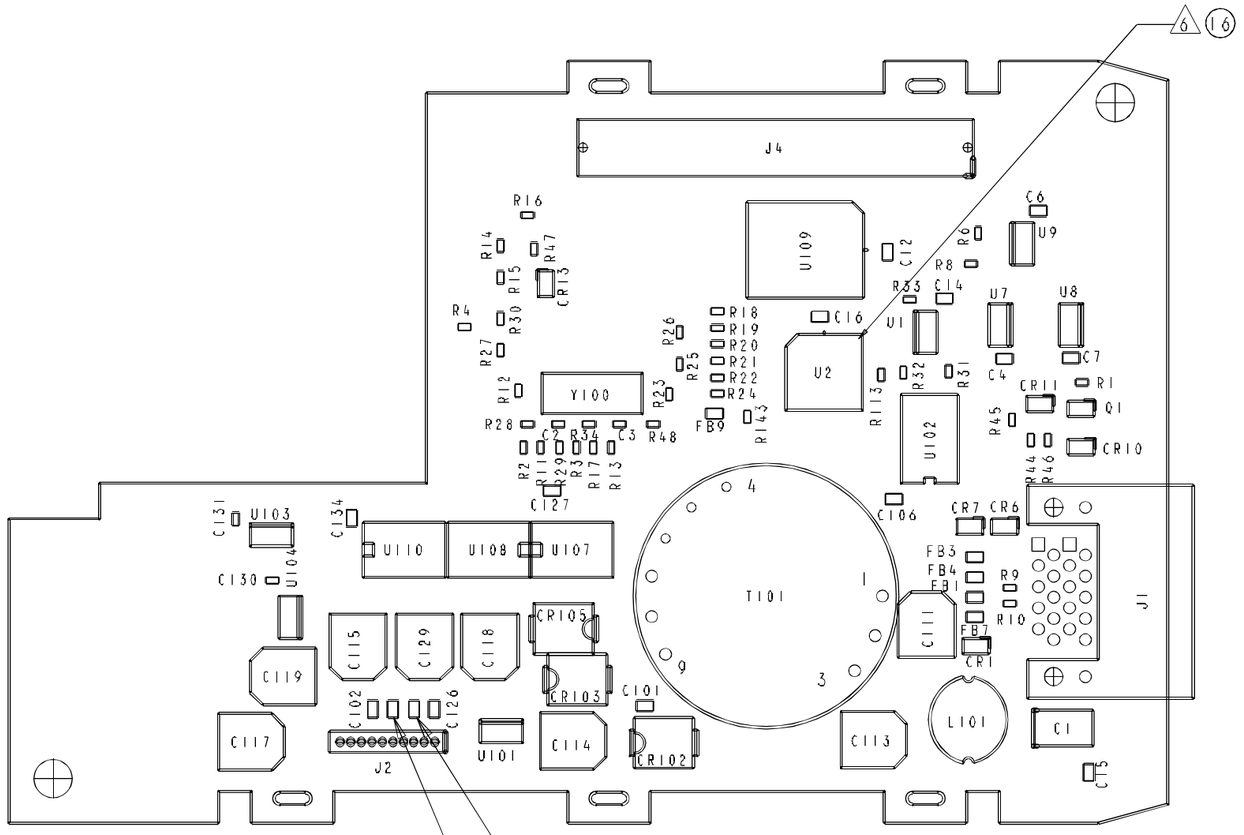
NOTES:

1. TORQUE TO 3 IN-LB ± 0.5 IN-LB.
2. TORQUE TO 4 IN-LB ± 0.5 IN-LB.
3. COAT THREADED FASTENERS WITH ADHESIVE BEFORE INSTALLATION.
4. ENCLOSURE TO BE ORIENTED WITH SMALLER GROOVE AT TOP.
5. TORQUE TO 6 IN-LB ± 1 IN-LB.
7. INSTALL SEQ NO. 48 OVER SEQ NO. 47 AS SHOWN IN VIEW B.
9. INSTALL USING PANDUIT GS2B CABLE GUN OR EQUIVALENT, SEETING-4 INT.
10. TO MEET PATIENT SAFETY REQUIREMENTS, VERIFY PROPER INSULATOR INSTALLATION. ENSURE THAT LONG NOTCH END IS TOWARD REAR OF MODULE.

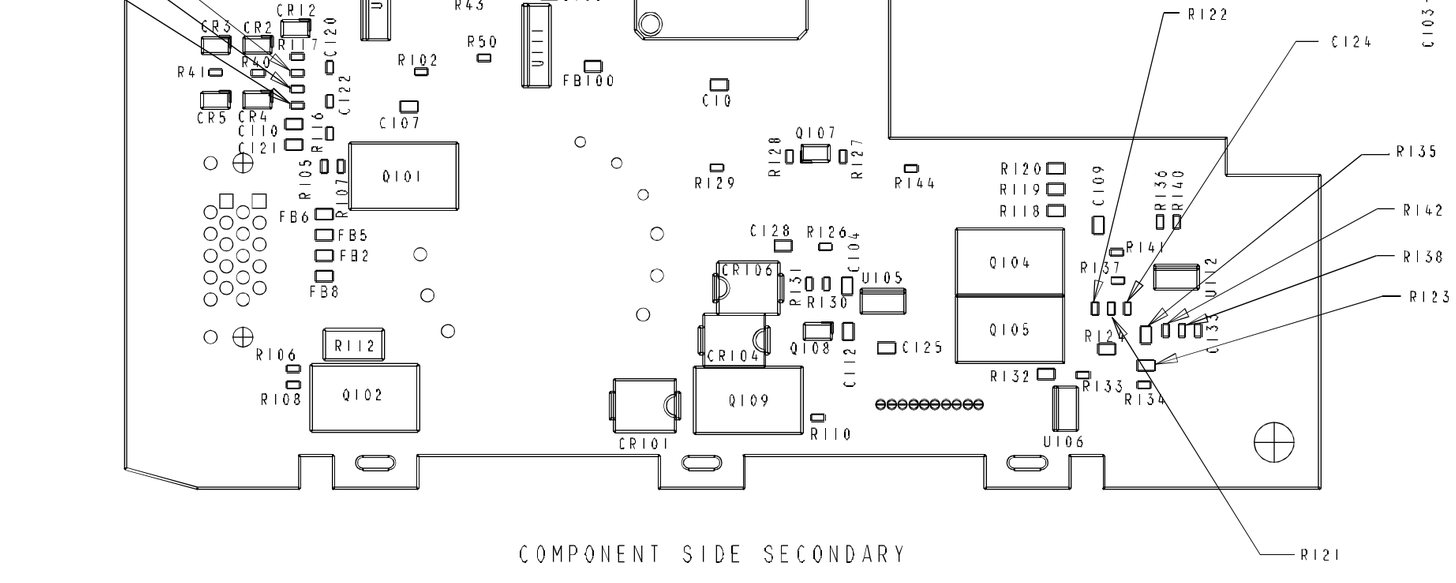
NOTES:

3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

⚠6 PROGRAM DEVICE PRIOR TO INSTALLATION.

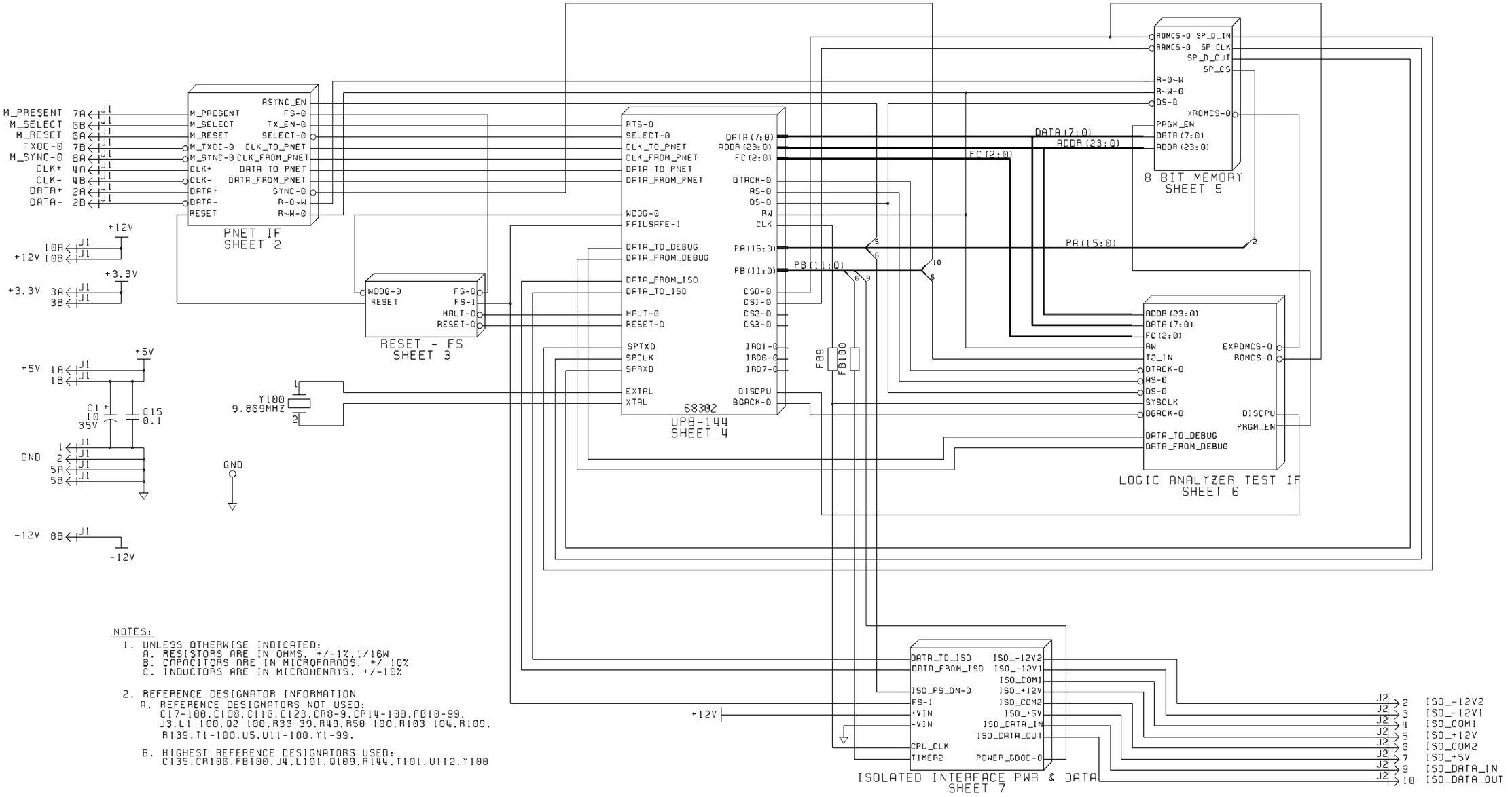


COMPONENT SIDE PRIMARY



COMPONENT SIDE SECONDARY

FO-7C. CO2 Digital PWA 315-446



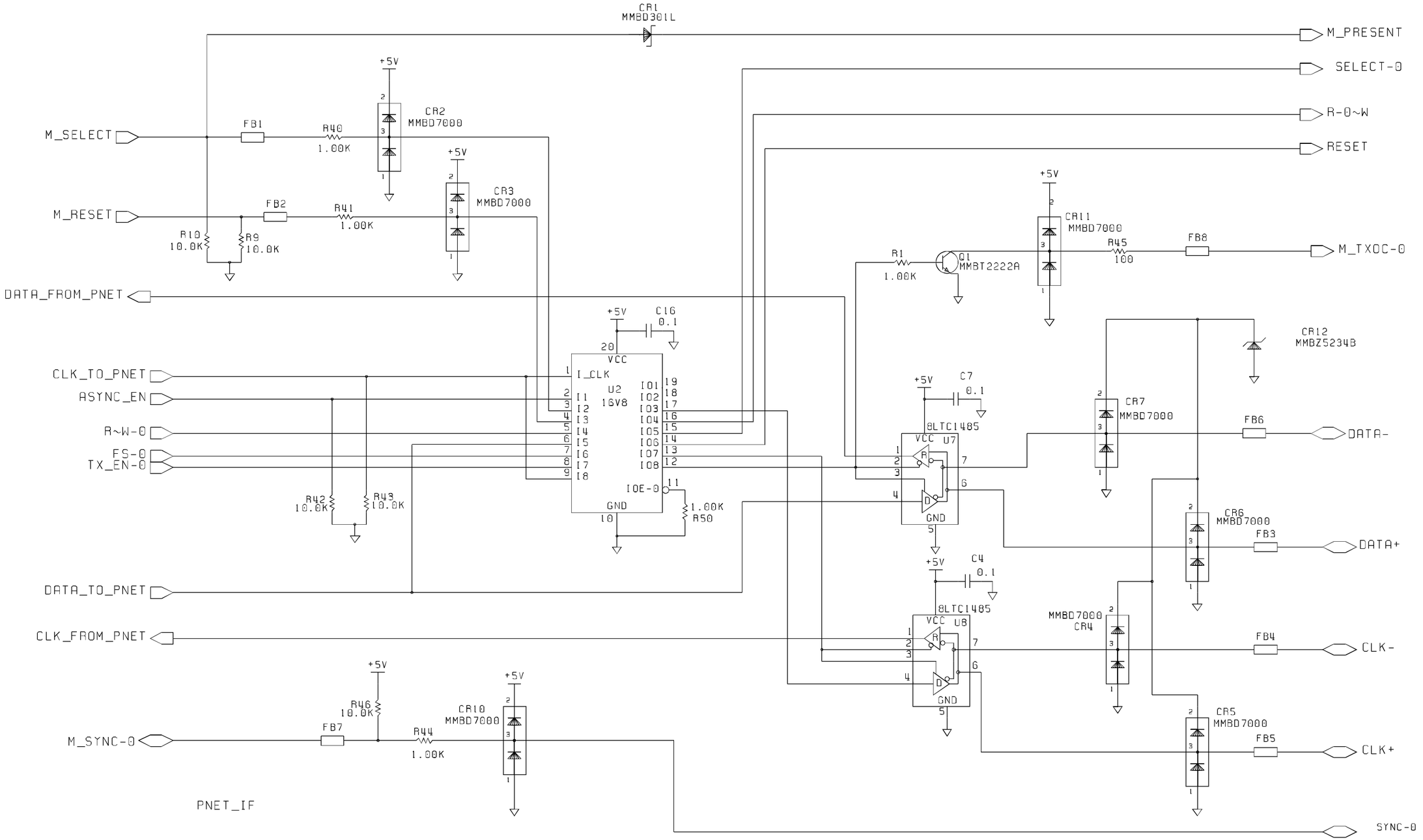
NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/16W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

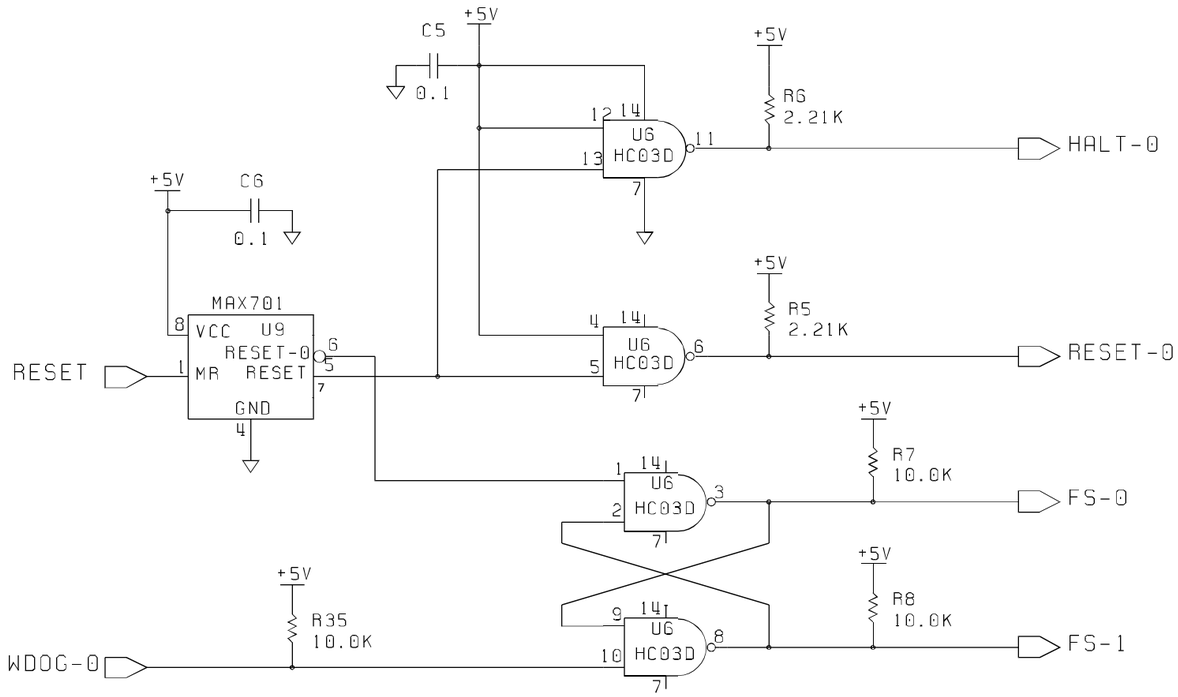
2. REFERENCE DESIGNATOR INFORMATION
   A. REFERENCE DESIGNATORS NOT USED:
      C17-100,C108,C116,C123,CR8-9,CR14-100,FB10-99,
      J3,L1-100,Q2-100,R36-39,R49,R50-100,R103-104,R109,
      R139,T1-100,U5,U11-100,Y1-99.

   B. HIGHEST REFERENCE DESIGNATORS USED:
      C135,CR106,FB100,J4,L101,Q109,R144,T101,U112,Y100

SC315-446 A
CO2 Digital PWA Schematic (1 of 7)

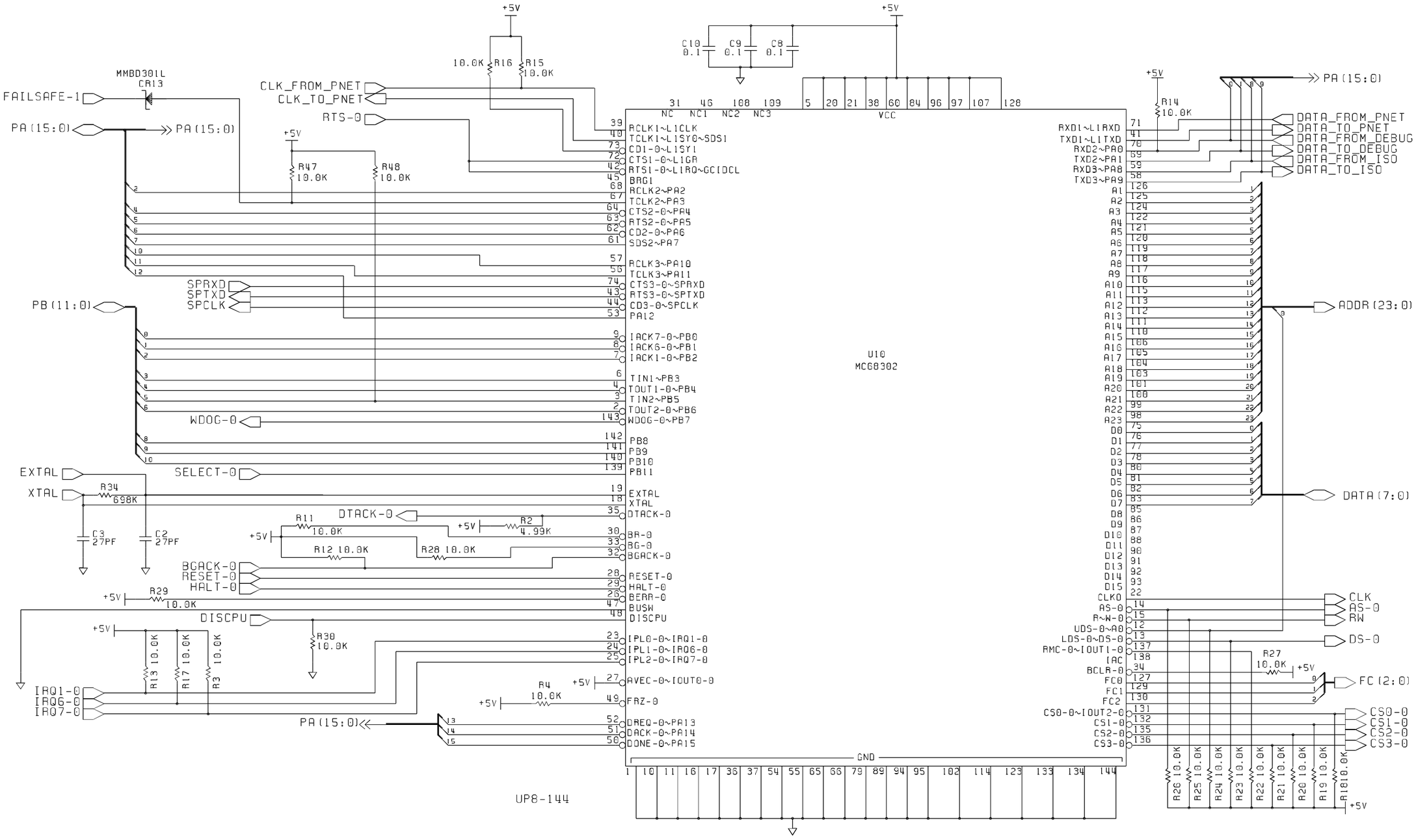


SC315-446 A
CO2 Digital PWA Schematic (2 of 7)

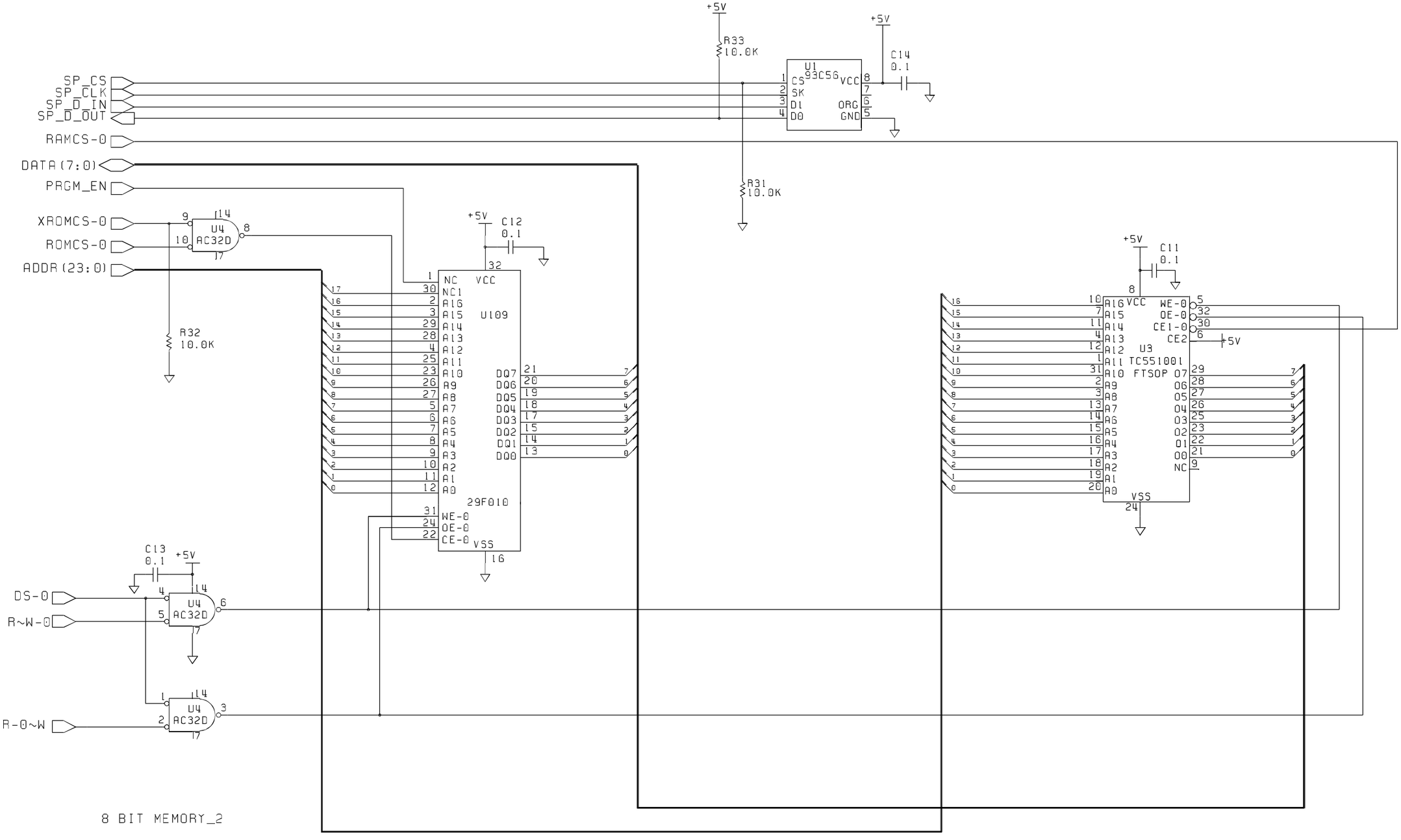


RESET - FS

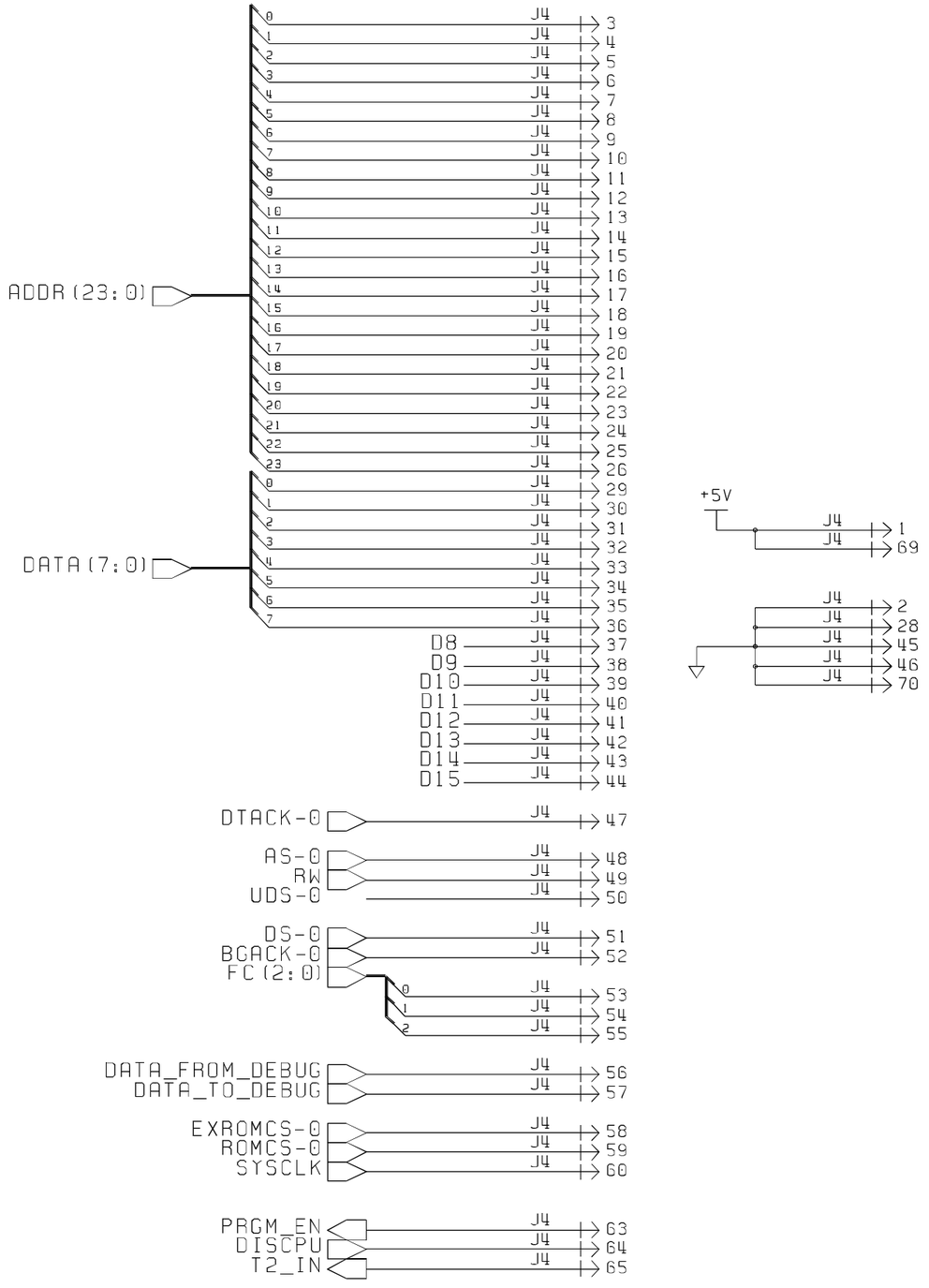
SC315-446 A
CO2 Digital PWA Schematic (3 of 7)



SC315-446 A
CO2 Digital PWA Schematic (4 of 7)

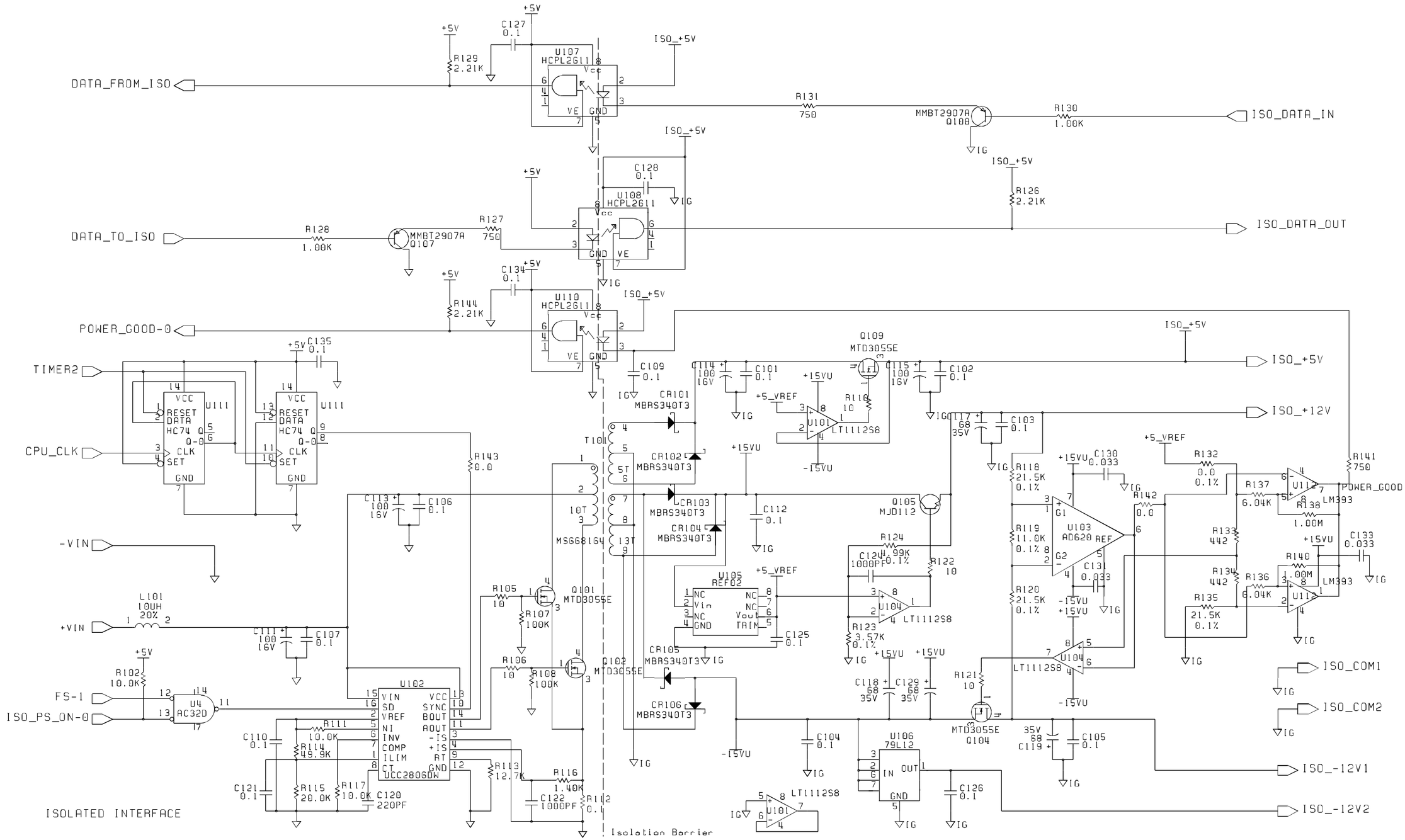


SC315-446 A
CO2 Digital PWA Schematic (5 of 7)



LOGIC ANALYZER TEST IF_4

SC315-446 A
CO2 Digital PWA Schematic (6 of 7)



SC315-446 A
CO2 Digital PWA Schematic (7 of 7)